Docket No.: F1866.0054
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masahiko Nakayama

Application No.: 09/705,050 Confirmation No.: 3890

Filed: November 2, 2000 Art Unit: 2124

For: FIR FILTER AND RAMP - UP/ - DOWN CONTROL CIRCUIT USING THE SAME Examiner: C. C. Do

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on August 5, 2004, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2), and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

10/06/2004 SDENBOB1 00000078 09705050
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This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

NEC Corp.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 20 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 1.

2. Claims withdrawn from consideration but not canceled: None.

3. Claims pending: 2-21.

4. Claims allowed: None.

5. Claims rejected: 2-21.

C. Claims On Appeal

The claims on appeal are claims 2-21.

IV. STATUS OF AMENDMENTS

Applicant filed an Amendment After Final on April 19, 2004. The Examiner responded in Advisory Action mailed on June 16, 2004, indicating that the amendments to claims 2-5, 7-10, and 17 would be entered. Applicant filed a Second Amendment After Final on July 14, 2004 that did not contain amended claims but did contain an argument

traversing the rejections. The Examiner responded in an Advisory Action mailed on August 26, 2004, indicating that the Amendment would be entered.

In addition, Applicant has corrected a typographical error in claim 1. As recited in Applicant's December 3, 2003 Amendment, claim 1 properly recites: "wherein a FIR filter output is derived from product outputs of the multiplying means." However, due to the typographical error, in the later April 19, 2004 Amendment After Final, claim 1 improperly recites: "wherein a FIR filter output is derived from the product outputs of the n multiplying circuits means." Applicant sets forth the correct language in Appendix A.

Accordingly, the claims enclosed herein as Appendix A incorporate the amendments made subsequent to final rejection.

V. SUMMARY OF INVENTION

The present invention relates to controlling the transmission power level of a transmission circuit in a radio transmitter / receiver. More particularly, it claims a Finite Impulse Response (FIR) filter employing a ramp-up/-down control circuit using the FIR filter.

As provided in the specification, it is customary for a CDMA transmitter to contain a digital section, analog section, and antenna. (See page 1, lines 24-26; Fig. 10.) A FIR filter for limiting bandwidth is disposed in the digital section. (See page 2, lines 1-2.) At the start and end of transmission (or upon burst transmission in TDMA), the spectrum of the transmission signal is spread, resulting in interference with other channels. (See page 2, lines 6-15.) Thus, a standard ramp-up and ramp-down time section is given for transmission data to limit channel interference. (See page 2, lines 18-20.)

In the conventional FIR filter, transmission data is shifted through an n-bit shift register and then fed through a memory into which is input a one-bit burst timing signal and clock. (See Fig. 11; page 2, lines 23-28 - page 3, lines 2-5.) As the tap number (number of shift register stages) increases, so do memory requirements and resulting overall circuit scale. (See page 3, lines 6-14.) In contrast to the prior art, the present invention enables better memory management and scalability while maintaining effective ramp-up /-down functionality.

Further, as distinguished from the prior art, the present invention claims a FIR filter wherein there is an n-to-n relationship between an n-bit shift register into which transmission data is fed and n switch elements that accept the output of such register. Additionally, again as distinguished from the prior art, the present invention claims a FIR filter including a switch element that is able to select either a fixed value or a FIR filter coefficient.

VI. ISSUES

Are claims 2, 4-7, 10, 14, 16-17, 19 and 21 patentable under 35 U.S.C. § 102(b) over Hidemitsu, J.P. 411088119A?

Are claims 3 and 11-12 patentable under 35 U.S.C. § 103(a) over Hidemitsu in view of Shinde, U.S. Patent No. 6,192,386?

Are claims 8-9, 13, 15, 18 and 20 patentable under 35 U.S.C. § 103(a) over Hidemitsu in view of Shinde in further view of the admitted prior art?

VII. GROUPING OF CLAIMS

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have been grouped as indicated below:

Group Claim(s)

I. 2-16.

II. 17-21.

VIII. ARGUMENT

In the Final Office Action mailed February 6, 2004, the Examiner finally rejected claims 2, 4-7, 10, 14, 16-17, 19 and 21 under 35 U.S.C. § 102(b) over Hidemitsu, J.P. 411088119A; claims 3 and 11-12 under 35 U.S.C. § 103(a) over Hidemitsu in view of Shinde, U.S. Patent No. 6,192,386; and claims 8-9, 13, 15, 18 and 20 under 35 U.S.C. § 103(a) over Hidemitsu in view of Shinde in further view of the admitted prior art.

There are three independent claims in the present application: 2, 10 and 17. For the following reasons, the rejections thereon under § 102 must be reversed. Further, the rejections on claims dependent thereon under §§ 102 and 103 must also be reversed.

A. Independent Claims 2 and 10 Are Patentable Over The Cited Art.

1. Claim 2 is Patentable Under § 102.

The Examiner rejected independent claim 2 under § 102(b) over Hidemitsu. This rejection is erroneous for the following reasons.

Independent claim 2 requires (emphasis added): a first ***n***-bit shift register, ***n***-switching means, ***n*** unique control signals, and a second ***n***-bit register. Hidemitsu does not show an ***n***-bit shift register, ***n*** switching means, ***n*** unique control signals, and a second ***n***-bit register.

In the rejection of claim 2 over Hidemitsu, the Examiner indicates that the implementation of Hidemitsu discloses: a first n-bit shift register in its elements 2-5 [thus, n = *4*] (Final Office Action, Second Advisory Action); n switching means 6-10 [thus, n = *5*] (Final Office Action, Second Advisory Action); n unique control signals S1-S5 [thus, n = *5*] (Final Office Action, First Advisory Action, Second Advisory Action); and a second n-bit register 108-113 [thus, n = *6*] (First Advisory Action).

Thus, in the implementation of Hidemitsu, n is simultaneously 4, 5 ***and*** 6. However, Applicant explicitly claims an "n-to-n-to-n-to-n" relationship. That is, "n" must be an identical value for each of the first n-bit shift register, n switching means, n unique control signals and second n-bit shift register. Hidemitsu shows "n" of 4, 5 and 6, which are not identical values.

Further, the Examiner indicates that Hidemitsu shows a first n-bit shift register where n=5. Applicant respectfully disagrees, because in Hidemitsu n = 4. As the Examiner admits in the Second Advisory Action (emphasis added):

> Hidemitsu discloses in Figure 7 an FIR filter comprising . . . a first n-bit shift register in particular n being a natural number n = 5 as x(1) . . . x(5) for progressively shifting the input data through successive stage bits (the data "IN" is shifting to the right ***into the register***), [and] n switching means (6-10) . . . .

As the Examiner indicates, data "IN", shown as item 1 in Hidemitsu, is shifted ***into the register*** shown as 2-5. "IN" itself is not part of the register. Based on Hidemitsu Fig. 7

and the Examiner's description thereof, the shift register has four bit-registers. Thus, n = 4.

For the reasons given above, independent claim 2 is patentable under § 102 over Hidemitsu, and the rejection thereon must be reversed. Further, the § 102 rejections as to claims 4-7 stand or fall with claim 2, on which they depend, and must also be reversed.

In addition, claims 3 and 8-9, which depend from claim 2, are patentable under § 103 over the cited art. Neither Hidemitsu, Shinde nor the admitted prior art teaches or suggests the n-to-n-to-n-to-n relationship described above, required in each of claims 3, 8 and 9. Thus, Shinde and the Admitted Prior Art do not cure the deficiencies of Hidemitsu. Applicant therefore respectfully submits that a *prima facie* case of obviousness has not been made out because the references, even if combined, do not teach each and every claim limitation. M.P.E.P. § 2143.

2. Independent Claim 10 is Patentable Under § 102.

The Examiner has rejected independent claim 10 under § 102(b) over Hidemitsu. This rejection is erroneous for the following reasons.

To begin, in the First Advisory Action, the Examiner stated that "claim 10 is also rejected under the same rationale in the rejection of rejected claim 2." The Examiner did not change this position in the Second Advisory Action. Because Applicant has shown that claim 2 is patentable over the cited art, and the Examiner indicated that claim 10 is rejected under the same rationale as that of claim 2, the rejection of claim 10 must be reversed.

Moreover, independent claim 10 requires (emphasis added): a first ***n***-bit shift register, ***n*** unique control signals, an ***n***-bit combining circuit, and ***n*** multipliers. Hidemitsu

does not show a first *n*-bit shift register, *n* unique control signals, an *n*-bit combining circuit, and *n* multipliers.

In the rejection of claim 10 over Hidemitsu, the Examiner indicates that Hidemitsu discloses: a first n-bit shift register in its elements 2-5 [thus, n = *4*] (Final Office Action, Second Advisory Action); n unique control signals S1-S5 [thus, n = *5*] (Final Office Action, First Advisory Action, Second Advisory Action); and n multiplying elements 11-15 [thus, n = *5*] (Final Office Action, Second Advisory Action). The Examiner does not identify where Hidemitsu contains the n-bit combining circuit as claimed, but simply states in the Final Office Action: "Re claim 10, it has the similar features stated in claim 1 [sic, 2]. Thus, claim 10 is also rejected under the same rationale in the rejection of rejected claim 1 [sic, 2]."

Thus, in the implementation of Hidemitsu, n is simultaneously 4 ***and*** 5. However, Applicant claims an n-to-n-to-n relationship. That is, as claimed, "n" must be an identical value for each of the first n-bit shift register, n unique control signals, and n multipliers. And again, the implementation of Hidemitsu shows "n" of 4 and 5, which are not identical values.

For the reasons given above, independent claim 10 is patentable over Hidemitsu under § 102, and the rejection thereon must be reversed. Further, the § 102 rejections as to claims 14 and 16 stand or fall with claim 10, from which they depend, and must also be reversed.

In addition, claims 11-13 and 15, which depend from claim 10, are patentable under § 103 over the cited art. Neither Hidemitsu, Shinde nor the Admitted Prior Art teaches or suggests the n-to-n-to-n relationship described above, required in each of claims 11-13 and 15. Thus, Shinde and the Admitted Prior Art do not cure the deficiencies of

Hidemitsu. Applicant therefore respectfully submits that a *prima facie* case of obviousness has not been made out because the references, even if combined, do not teach each and every claim limitation. M.P.E.P. § 2143.

B. Independent Claim 17 is Patentable Over The Cited Art.

The Examiner has rejected independent claim 17 under § 102(b) over Hidemitsu. This rejection is erroneous for the following reasons.

Nowhere does Hidemitsu show, as required by claim 17, a FIR filter including (emphasis added): "a switch coupled to the control circuit, coupled to the fixed value circuit and coupled to the FIR filter coefficient circuit, each switch selecting either the fixed value ***or*** the FIR filter coefficient . . . ." Hidemitsu fails to teach or suggest a switch that can select a FIR filter coefficient.

None of Figures 1, 7 and 11 of Hidemitsu, referenced by the Examiner, shows that a FIR filter coefficient value is an input to any switch. The switches shown in Hidemitsu either switch between the data and 0 (Figure 1), or between the data and a code converter that merely appears to invert the value of the delay element (Figure 7); further, Figure 11 does not disclose any switches whatsoever. Thus, Hidemitsu nowhere teaches or suggests a switch that can select "either the fixed value or the FIR filter coefficient", as required by claim 17 of the present invention.

For the reasons given above, independent claim 17 is patentable over Hidemitsu under § 102, and the rejection thereon must be reversed. Further, the § 102 rejections as to claims 19 and 21 stand or fall with claim 17, on which they depend, and must also be reversed.

In addition, claims 18 and 20, which depend from claim 17, are patentable under § 103 over the cited art. Neither Hidemitsu, Shinde nor the Admitted Prior Art teaches or suggests a switch that can select "either the fixed value or the FIR filter coefficient", as required by claim 17 of the present invention. Thus, Shinde and the Admitted Prior Art do not cure the deficiencies of Hidemitsu. Applicant therefore respectfully submits that a *prima facie* case of obviousness has not been made out because the references, even if combined, do not teach each and every claim limitation. M.P.E.P. § 2143.

IX. CLAIMS INVOLVED IN THE APPEAL

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A include the amendments filed by Applicant on April 19, 2004.

Dated: October 5, 2004

Respectfully submitted,

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/705,050

1. (Canceled)

2. (Previously presented): A Finite Impulse Response (FIR) filter comprising:

a selection control means for selecting input data, the selection control means including:

a first n-bit shift register (n being a natural number) for progressively shifting the input data through successive stage bits,

n switching means respectively provided for outputs of the n stage bits of the n-bit shift register for controlling the outputs of these n bits, and

a control means for controlling the n switching means, the control means outputting n unique control signals respectively to the n switching means, the control means further being constituted by a second n-bit shift register for shifting a ramp-up/-down signal through successive bit stages under control of a shift clock for the first n-bit shift register; and

a multiplying means for multiplying data selected by the selection control means and a predetermined filter coefficient,

wherein a FIR filter output is derived from product outputs of the multiplying means.

3. (Previously presented): The FIR filter according to claim 2, wherein:

the n switch means are each an AND gate for receiving the outputs of the corresponding bit stages of the first and second n-bit shift registers as respective inputs.

4. (Previously presented): The FIR filter according to claim 2, wherein: the n switching means are n switches provided for bit stages of the second n-bit shift register for selectively feeding out the filter coefficient data and zero data in response to the outputs of the corresponding bit stages.

5. (Previously presented): The FIR filter according to claim 2, wherein the outputs of the bit stages of the first n-bit shift register are reset on the basis of the outputs of the corresponding bit stage of the second n-bit shift register.

6. (Previously Presented) The FIR filter according to claim 2, which further comprises a means for changing a shift clock frequency of the first n-bit shift registers.

7. (Previously presented): The FIR filter according to claim 2, wherein the shifting operation of the first and second n-bit shift registers are operated under control of shift clock signals at different frequencies.

8. (Previously presented): The FIR filter according to claim 3, further comprising an adder circuit for adding together the outputs of the n multiplying circuits, wherein a ramp-up signal is fed to the first n-bit shift register, the ramp-up data being derived from the sum output of the adder circuit.

9. (Previously presented): The FIR filter according to claim 3, further comprising an adder circuit for adding together the outputs of the n multiplying circuits,

wherein a ramp-down signal is fed to the first n-bit shift register, the ramp-down data being derived from the sum output of the adder circuit.

10. (Previously presented): A Finite Impulse Response (FIR) filter comprising:

a first n-bit shift register that receives an input signal and outputs n first-register output signals;

a control circuit that outputs n unique control signals;

an n-bit combining circuit coupled to the first n-bit shift register and coupled to the control circuit, the combining circuit combining the n output signals of the first n-bit shift register with the n unique control signals of the control circuit, the n-bit combining circuit outputting a combining circuit output signal;

n multipliers coupled to the n-bit combining circuit, each of the multipliers multiplying the combining circuit output signals with n filter coefficients, each of the n multipliers outputting a product; and

an adder coupled to the n multipliers, the adder adding the products of the n multipliers.

11. (Previously presented): The FIR filter according to claim 10, wherein the combining circuit consists of n logic gates.

12. (Previously presented): The FIR filter according to claim 11, wherein the logic gates are AND gates.

13. (Previously presented): The FIR filter according to claim 10, wherein an input to the control circuit is a ramp-up/ramp-down signal.

14. (Previously presented): The FIR filter according to claim 10, wherein the control circuit includes a second n-bit shift register.

15. (Previously presented): The FIR filter according to claim 14, wherein an input to the control circuit is a ramp-up/ramp-down signal.

16. (Previously presented): The FIR filter according to claim 10, further comprising:

a second clock signal supplied to the first n-bit shift register; and

a first clock signal supplied to the control circuit;

wherein the second clock signal has a different frequency than the first clock signal.

17. (Previously presented): A Finite Impulse Response (FIR) filter comprising:

a first n-bit shift register that receives an input signal and outputs a first-register output signal;

a control circuit that outputs n unique control signals;

n switching circuits, each switching circuit comprising:

a circuit for producing a fixed value;

a circuit for producing a FIR filter coefficient;

a switch coupled to the control circuit, coupled to the fixed value circuit and coupled to the FIR filter coefficient circuit, each switch selecting either the fixed value or the FIR filter coefficient depending upon the control circuit output signal, outputting a switch selection output;

a multiplier coupled to the switch and coupled to the first n-bit shift

register, the multiplier multiplying the switch selection output with a selected one of the n first-register output signals to produce a switching circuit output; and

an adder coupled to the n switching circuits, the adder adding the outputs of the n switching circuits.

18. (Previously presented): The FIR filter according to claim 17, wherein an input to the control circuit is a ramp-up/ramp-down signal.

19. (Previously presented): The FIR filter according to claim 17, wherein the control circuit includes a second n-bit shift register.

20. (Previously presented): The FIR filter according to claim 19, wherein an input to the control circuit is a ramp-up/ramp-down signal.

21. (Previously presented): The FIR filter according to claim 17, further comprising:

a second clock signal supplied to the first n-bit shift register; and

a first clock signal supplied to the control circuit;

wherein the second clock signal has a different frequency than the first clock signal.

AF #

PTO/SB/17 (10-03)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 340.00

Complete if Known	
Application Number	09/705,050-Conf. #3890
Filing Date	November 2, 2000
First Named Inventor	Masahiko Nakayama
Examiner Name	C. C. Do
Art Unit	2124
Attorney Docket No.	F1866.0054

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☒ Credit Card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account:

Deposit Account Number: 50-2215

Deposit Account Name: Dickstein Shapiro Morin & Oshinsky LLP

The Director is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims	20	-20** =	0	x	18.00	=	0.00
Independent Claims	3	-3** =	0	x	9.00	=	0.00
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	340.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
Other fee (specify)					

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 340.00

SUBMITTED BY

(Complete *(if applicable)*)

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Signature	Michael J. Scheer			*Date*	October 5, 2004